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Attorney Docket SEL 171

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Kadono et al.

Serial No.: 09/535,233

Filed: March 24, 2000

For: A Method Of Manufacturing A Semiconductor Device

Art Unit: 2823

Examiner: W. Coleman

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August 17 2004
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Shannon Wallace
Name of applicant, assignee, or Registered Rep.

Shannon Wallace 8/17/04
Signature Date

Commissioner for Patents
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Sir:

RESPONSE G (AFTER FINAL)

Applicants have the following response to the Final Rejection dated May 17, 2004.

REMARKS

Claim Rejections - 35 USC §103

In the Final Rejection, the Examiner continues to reject Claims 11-18 under 35 USC §103 as being unpatentable over Lin et al. in view of Muraoka et al. The Examiner also continues to reject Claims 13, 14, 17 and 18 under 35 USC §103 as being unpatentable over Lin et al. in view of Muraoka et al. and further in view of Araujo. The Examiner also continues to reject Claims 19, 20, 23, 24, 27 and 28 under 35 USC §103 as being unpatentable over Lin et al. in view of Muraoka et al. and Yoshikawa. The Examiner also continues to reject Claims 21, 22, 25, 26, 29 and 30 under 35

USC §103 as being unpatentable over Lin et al. in view of Muraoka et al. and Yoshikawa et al. and further in view of Araujo et al.

Each of these rejections is respectfully traversed.

For example, independent Claim 11 recites *forming a gate insulating film in contact with the semiconductor film from the surface of which the contaminating impurity has been removed.* A similar feature is recited in independent Claims 11 and 15. This feature is not disclosed in any of the cited references.

The Examiner admits that Lin fails to teach this feature but cites Muraoka. Muraoka teaches that the treatment of a silicon wafer with an oxidizing acid results in the formation of a very thin oxide film on the surface of the wafer. The Examiner seems to regard the very thin oxide film as a gate insulating film.[1] Applicants respectfully disagree as the very thin oxide film has a role of absorbing the metal impurity, but not a role as a gate insulating film (see e.g. col. 2, lns. 45-58).

Further, while Muraoka discloses that the surface of a silicon wafer comprises silicon and silicon oxide used as a gate oxide film of, for example, a transistor, Muraoka teaches that the gate oxide film is etched by etchant (see e.g. col. 4, lns. 55-56). Hence, etching is performed **after** forming the gate oxide film. In contrast, in the claimed invention, spin-etching is performed **before** forming the gate insulating film.

Applicants have previously advised the Examiner of this distinction. However, in the section "Response to Arguments" in the Final Rejection, the Examiner has not addressed this distinguishing feature of the claimed invention.

Applicants respectfully submit that this is a distinguishing feature of the claimed invention that is not disclosed or suggested by the cited references. If the Examiner disagrees, it is respectfully

[1] The Final Rejection, however, is very vague as to where the Examiner believes the claimed features are shown in Muraoka.

requested that he specifically identify where in the cited references this feature is shown.

With regard to Claims 23 and 27, these claims recite *forming a gate insulating film and a semiconductor film over the gate wiring after the contaminating impurities are removed from the surface of the substrate.* This feature is also not disclosed by the cited references.

In the Final Rejection, the Examiner contends that the gate electrodes are inherent in the formation of an electrode and one of the fundamental parts of a MOS system as allegedly disclosed by Muraoka (col. 1, ln. 53) and that Yoshikawa teaches that the electrode layer can be the gate wiring layer.

Applicants respectfully disagree with the Examiner's contention. Yoshikawa does not disclose or suggest a gate electrode. Even if a gate electrode was arguably inherent, none of the cited references teach the above claimed feature. Further, in the section "Response to Arguments" in the Final Rejection, the Examiner has not addressed this distinguishing feature of the claimed invention.

Applicants respectfully submit that this is a distinguishing feature of the claimed invention that is not disclosed or suggested by the cited references. If the Examiner disagrees, it is respectfully requested that he specifically identify where in the cited references this feature is shown.

Interview Request

The undersigned requests an interview with the Examiner to discuss each of the above features and where they are allegedly disclosed in the cited references. The undersigned will call the Examiner to set up the interview.

Conclusion

Hence, the method of the claimed invention is not disclosed or suggested by the cited

references.

Therefore, for at least the reasons discussed above, the claims of the present application are patentable over the cited references and should now be allowed.

Please charge Deposit Account No. 50-1039 for any fee for this submission.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: August 17, 2004

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